CHARACTERIZATION OF GaAs DEVICES BY A VERSATILE PULSED I-V MEASUREMENT SYSTEM

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ABSTRACT

We have built and utilized a pulsed I-V system which is capable of reaching any current-voltage point of three-terminal devices from any arbitrarily chosen DC bias point. The system, which can be used on wafer, serves as an invaluable tool for device modeling and process diagnostics. Direct dependence of the pulsed I-V curves on the DC bias was found in GaAs MESFETs and HEMTs.

INTRODUCTION

The families of the source-drain and the gate-drain breakdown I-V curves, parameterized by the gate voltage, of GaAs FET devices (both MESFETs and HEMTs) underlie the performance of such devices. It is common knowledge that these curves are affected by the channel temperatures of the devices and by the frequency at which the data is taken. Curve tracer or parameter analyzer curves do not adequately characterize the performance of both small periphery devices, used for small signal gain applications, and large periphery power devices. In the former case, the performance at a fixed DC bias is an important concern as well as the current and voltage excursions between the open channel current and the gate-drain breakdown voltage, in the latter case. In particular, it has been observed that both g_m and R_{ds}, which can be calculated, in principle, from these curves, do not agree with values obtained from S-parameter measurements performed at frequencies higher than 10-100 MHz. It has also been observed that quite often power devices do not deliver as much power at microwave frequencies as would be expected from their DC I-V curves. Frequency effects are often attributed to bulk and/or surface states or traps.[1-2]

To overcome both temperature and frequency effects in characterizing devices, several authors have suggested either measuring the I-V curves at 1-10 MHz [3-4], or pulsing either the gates or the drains with short pulses [5-8] typically 200-500 nS long at low duty cycles. The effect of the DC bias on the behavior of the devices was considered only as far as it affected their channel temperatures. Other direct effects were not considered or investigated.

We postulated that GaAs FETs have slow states that are set by the DC bias and cannot respond to rapid signal changes; and therefore, the DC bias has a direct and dramatic effect on both the I-V curves and device behavior. We want to report in this paper that this is indeed the case. Furthermore, we want to report a novel pulsed measuring system that measures I-V curves that are quite different from those obtained from standard curve tracers or parameter analyzers. These I-V curves serve as a basis for simulation of large and small signal device performance; in particular, the small signal parameters that can be derived from them agree very well with S-parameters measurements.

PULSED I-V MEASUREMENT SYSTEM

To fully investigate three-terminal devices (MESFETs, HEMTs and HBTs), we constructed a versatile pulsing system which is capable of applying simultaneously both Gate (base) and drain (collector) pulses to such devices. The pulsing system (schematic shown in Figure 1) is capable of applying both positive and negative pulses superimposed on fixed DC levels and is thus capable of reaching any point on the I-V plane from any arbitrary DC bias point. The pulses, which can be applied at repetition rates in the range of 20 HZ to 1 MHz,

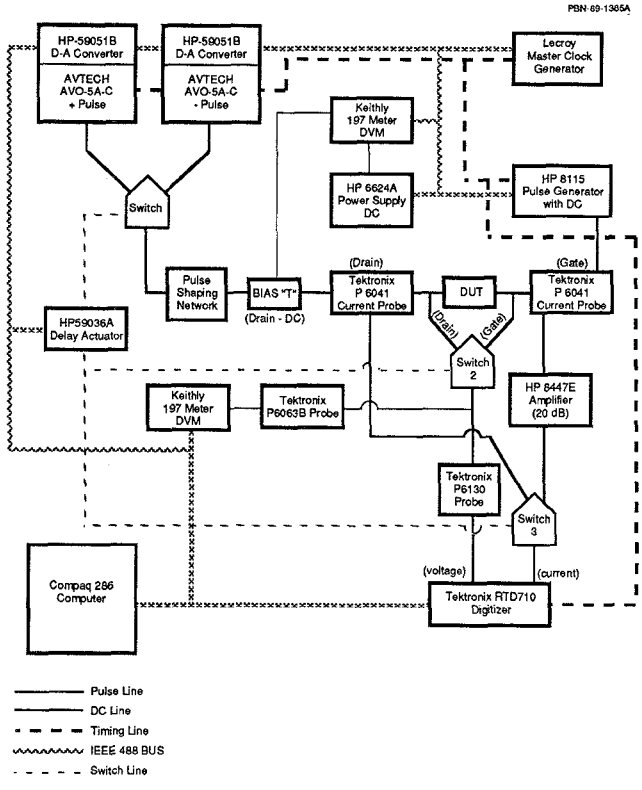

Figure 1. Block Diagram of Pulsed I-V System.

are 200 nS long with a rise time of 5nS and a settling time of 50 nS. The voltage and current capabilities of the drain pulsers are 20 V and 2 A respectively. The gate pulser is capable of delivering ±8 V across 50 Ω, for a maximum current of 160 mA. The gate and drain currents are sensed by inductive pick-up probes while the voltages are sensed by high impedance probes.

The system is fully under software control. Both the hardware and the custom software were designed to ensure that the devices can be driven to their full range of interest without blowing up under testing. To that end, the pulses are specially shaped to avoid leading and trailing spikes; the gate and drain pulses are always applied in the proper sequence, and the currents and power dissipations limits of the devices are properly sensed and never exceeded.

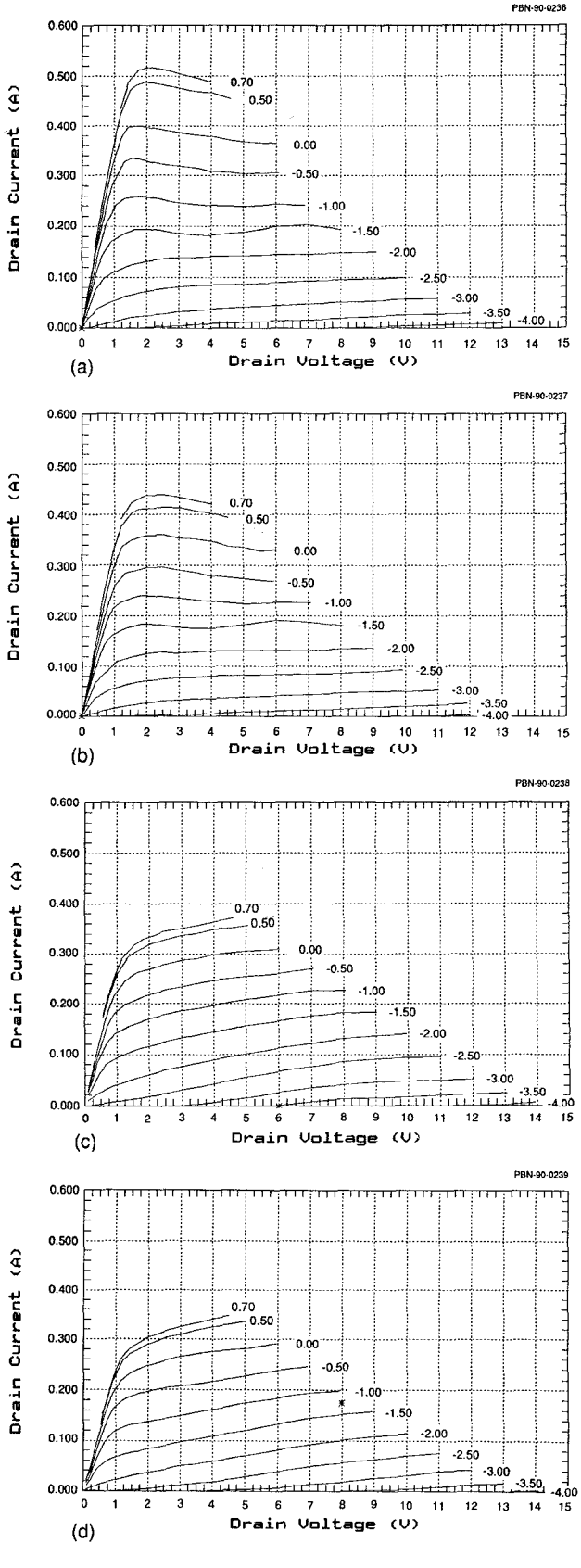

Figure 2. Pulsed I-V Curves of a 1.2 mm Ion-Implanted GaAs MESFET From Different DC Bias Points. (a) V_{ds} = 0 V, V_{gs} = 0 V, (b) V_{ds} = 0 V, V_{gs} = -4 V, (c) V_{ds} = 6 V, V_{gs} = -4 V, (d) V_{ds} = 8 V, V_{gs} = -1.25 V. All curves parameterized by V_{gs}.

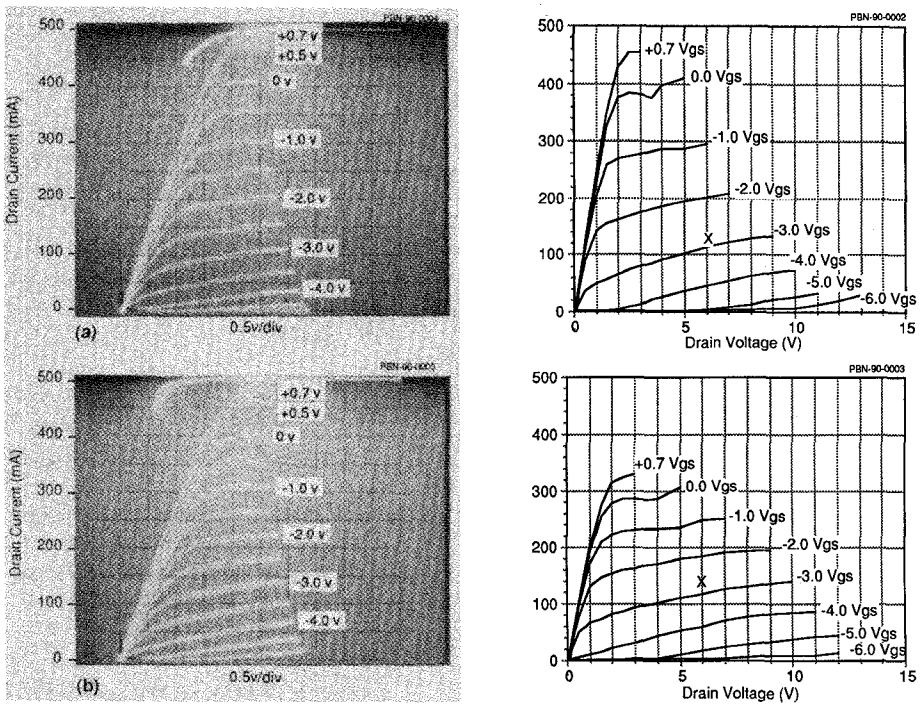

Figure 3. Curve Tracer and Pulsed I-V Curves of Passivated (a) and Nonpassivated (b) 1.2 mm Ion-Implanted GaAs MESFETs. Pulsed I-V measured from a DC bias of V_{ds} = 6 V, V_{gs} = -2.5 V.

RESULTS

Some of the more interesting results obtained by our pulsed I-V system are shown in Figures 2-5. In all cases, we pulsed 1.2 mm periphery, 0.5 μm gate length ion-implanted GaAs MESFET devices. Figure 2 clearly shows the dramatic effect of the DC bias on the pulsed I-V curves. Drastic changes are seen in both amplitudes and shapes of the curves as we move from (a) to (b) to (c). Notice that in all three cases the DC dissipation is equal to zero and the channel temperatures are expected therefore to be the same. Temperature effects can be seen by comparing (c) to (d). The general shape of the curves remain unchanged and the magnitudes decrease somewhat due to the higher channel temperature brought about by the DC dissipation in (d).

Figure 3 shows the effects of surface states or charges on the characteristics of ion-implanted GaAs MESFETs. Both devices were processed on the same wafer until the Si_3N_4 passivation step at which point the wafer was cleaved. Half a wafer was passivated while the other half was not. The device shown in Figure 3(a) was passivated, the one in (b) was not.

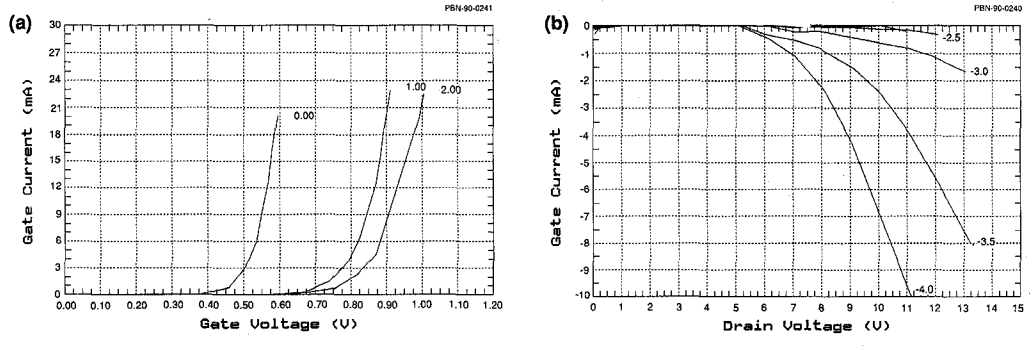

Figure 4. Forward (a) and Breakdown (b) Pulsed Gate Currents of 1.2 mm Ion-Implanted GaAs MESFETs. DC bias is V_{ds} = 8 V, V_{gs} = -1 V. Figure (a) parameterized by V_{ds}, (b) parameterized by V_{gs}.

The left parts of Figure 3 show that the conventional curve tracer I-V curves of both devices are quite similar. Drastic differences, however, are evident on the right sides of the figure where we show the pulsed I-V curves taken from a DC bias of V_{ds} = 6 V, V_{gs} = -2.5 V. The same two devices were assembled into microwave jigs and power tuned at 10 GHz. The nonpassivated device performed very badly. At the stated bias, the passivated device delivered 27.7 dBm while the other device delivered only 25.8 dBm. It should be noted that the nonpassivated device has a somewhat higher breakdown voltage as shown in the top traces of the curve tracer pictures.

The pulsed, forward and reverse (breakdown), gate currents, parameterized by V_{ds} and V_{gs} respectively, are shown in Figure 4. It is interesting to note that the breakdown curves increase only moderately and do not show the expected exponential increases.

Finally, Figure 5 shows the measured and simulated performances of a power device biased at V_{ds} = 8 V, V_{gs} = -1 V and power tuned at 10 GHz. The pulsed I-V curves were fitted to the Materka [9] model. The reactive elements were extracted from conventional small signal S-parameter measurements at the DC bias point. The performance was simulated on Microwave HARMONICA®. The small signals g_m and R_{ds} agree very well with the values obtained from the fitted Materka model and the large signal simulation coincides in the limit of low input power with the small signal behavior as predicted from the S-parameters. No external fixes were needed.

REFERENCES

1. T.M. Burton, P.H. Ladbrooke, "Low-Field Low-Frequency Dispersion of Transconductance in GaAs MESFETs with Implications for Other Rate-Dependent Anomalies", IEEE Trans. ED, Vol. 35, No. 3, 1988, pp. 257-267.

2. T.M. Barton, P.H. Ladbrooke, "The Role of the Device Surface in the High Voltage Behavior of the GaAs MESFET", Solid-State Elect., Vol. 29, No. 8, 1986, pp. 807-813.

3. M.A. Smith, T.S. Howard, K.J. Anderson, T.M. Pavio, "RF Nonlinear Device Characterization Yields Improved Modeling Accuracy", MTT-S Digest, 1986, pp. 381-384.

4. C. Camacho-Penalosa, C.S. Aitchison, "Modelling Frequency Dependence of Output Impedance of a Microwave MESFET at Low Frequencies", Elect. Letts., Vol. 21, No. 12, 1985, pp. 538-539.

5. M. Paggi, P.H. Williams, J.M. Borrego, "Nonlinear GaAs MESFET Modeling Using Pulsed Gate Measurements", IEEE Trans. MTT, Vol. 36, No. 12, 1988, pp. 1593-1597.

6. T.M. Burton, C.M. Snowden, J.R. Richardson, "Narrow Pulse Measurements of Drain Characteristics of GaAs MESFETs", Elect. Letts., Vol. 23, No. 13, 1987, pp. 686-687.

7. G. Halkis, H. Gerard, Y. Crosnier, G. Salmer, "A New Approach to the RF Power Operation of MESFETS", IEEE Trans. MTT, Vol. 37, No. 5, 1989, pp. 817-825.

8. J.F. Vidalou, F. Grossier, M. Camiade, J. Obergon, "On-Wafer Large Signal Pulsed Measurements", MTT-S Digest, 1989, pp. 831-834.

9. A. Materka, T. Kacprzak, "Computer Calculation of Large-Signal GaAs FET Amplifier Characteristics", IEEE Trans. MTT, Vol. 33, No. 2, 1985, pp. 129-135.

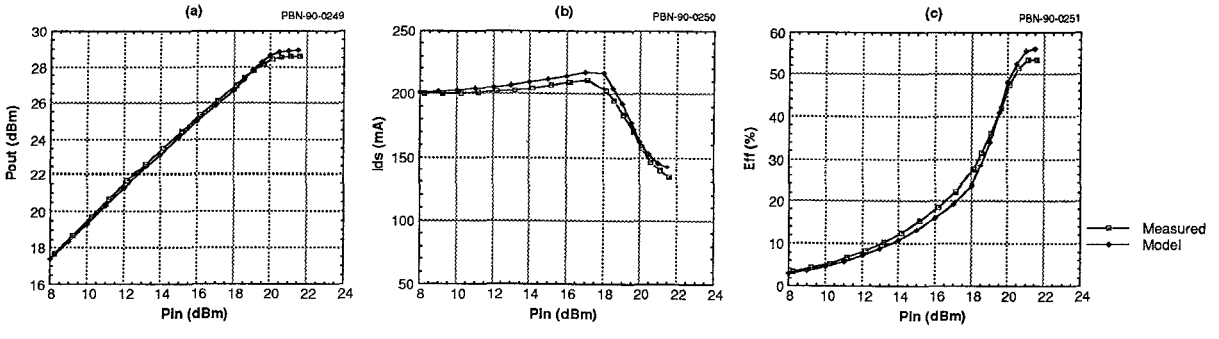

Figure 5. Measured and Modeled 10 GHz Tuned Performance of a 1.2 mm Ion-Implanted GaAs MESFET. (a) output power, (b) DC drain current, (c) Power added efficiency. DC bias is V_{ds} = 8 V, V_{gs} = -1 V.